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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/698,247	10/30/2000	Sghaier Noury	BONN-039	6242

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EXAMINER
SHAAWAT, MUSSA

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/698,247	NOURY ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is responsive to the application filed on October 30, 2000. Claims 1-13 are presented for examination.

Oath/Declaration

The citizenship is not identified for each inventor in the declaration. Appropriate action is required.

Claim objections

1. The applicant mentions "SSRAM memory" in (claim 10 line 4) no known definition for SSRAM memory in the art; it appears to be a spelling typo, the examiner interprets SSRAM memory to be SRAM memory. Appropriate action is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claim 1 recites the limitation "said device being characterized" in, claim 1 line 4. There is insufficient antecedent basis for this limitation in the claim.

3. Claim 3 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant mentions the phrase "a so-called internal bus" in claim 3 line 2 the language in the claim is indefinite.

4. Regarding claim 11, the phrase "for example" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

5. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Appropriate action is required.

Claim Rejections - 35 USC § 102

> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Asano et al. US Patent No. (5,572,710) referred to hereinafter as Asano.

7. As per claim 1 a real time functional replicator (10) of a specific integrated circuit comprised of a processing unit and peripherals in order to perform specific digital and/or analog functions controlled by specific application, the specific integrated circuit being designed to be incorporated into a specified application board; the device being characterized in that it includes, see Asano (Abstract, col.1, lines 35-67, col.3, lines 55-60, and col.4, lines 3-15): a processing module (12) that is functionally identical to the processing unit of the specific integrated circuit, see Asano (col.3, lines 50-67, col.13, lines 15-67); a plurality of peripheral modules (14, 16, 1s) each able to implement mw or more digital and/or analog functions, each of the functions being able to be selected separately, see Asano (col.20, lines 15-40, col.26, lines 1-8); and function interconnection means (20) for establishing the connections between the processing module one ore more digital and/or analog functions previously selected and located in at least one of the peripheral modules, the functions being identical to the specific functions of the specific integrated circuit such that the replicator behaves identically to the specific integrated circuit when the specific software is run, see Asano (col.4, lines 50-51, col.7, lines 45-54, col.12, lines7-10 , col.12, 12-40, and col.20, lines 15-30,).

8. As per claim 2 the device according to claim 1, wherein the function interconnection means are included in a standalone module (20), see Asano (col.11, lines 23-35).

9. As per claim 3 the device according to claim 2, in which the function interconnection module (20) is connected to the processing module (12) through a so-called internal bus (28) grouping together the internal connections of the specific integrated circuit between its processing unit and its peripherals, see Asano (col.7, lines 45-54, col.11, lines 23-34, col.12, and line 7-45, col.20, lines 13-30).

10. As per claim 4 the device according to claim 2, in which the function interconnection module (20) is configured by a programmable automaton (44) using software set up when the digital and/or analog functions, which must be implemented by the peripheral modules (14,16,18), have been selected, see Asano (col.11, lines 23-34).

11. As per claim 5 the device according to claim 1wherein the interconnection means are integrated within the peripheral modules (14. 16, 1 8), see Asano (col.12, lines 7-45, and col.20, lines 13-30).

12. As per claim 6 the device according to claim 1, in which the peripheral modules feature one or more integrated circuits (14, 16) each of which are specially designed to implement a plurality of digital and/or analog functions, see Asano (col.20, lines 20-42, col.25, lines 15-20, and col.26 lines 1-8).

13. As per claim 7 the device according to claim 6, in which the peripheral modules also include one or more FPGA type programmable logic arrays (13) which were previously programmed to implement at least one digital function which is not implemented by the

integrated circuits (14, 16) specially designed to implement the digital and/or analog functions, see Asano (col.7, lines 45-55, col.4, line 64-65).

14. As per claim 8 the device according to claim 7, featuring an input/output connection module (22) and an interface (24) connected to the input/output interconnection module by an input/output bus (34) and which can be connected to the input/output pins of the specific integrated circuit in the specified application board, the input/output interconnection module establishing the connections between the outputs of the digital and/or analog functions previously selected of the peripheral modules (14, 16, 12) and the interface, see Asano (col.3, lines 25-47, and col.6, lines 55-60).

15. As per claim 9 the device according to claim 7 in which the input/output interconnection module (22) is configured by the programmable automaton (44) by means of the software set up when the digital and/or analog functions were selected, see Asano (col.11, lines 23-41).

16. As per claim 10 the device according to claim 1 further including a ROM emulation module (45) connected directly to the processing module (12) to emulate the ROM memory of the specific integrated circuit the ROM emulation module preferably being a SRAM memory, having the same type of access and the same access time as the ROM memory see Asano (col.7, lines 55-63).

17. As per claim 11 the device according to claim 10, used as an emulation device of the specific integrated circuit when the interface (24) is connected, for example, using a ribbon cable (36), to the input/output pins of the specific integrated circuit (27) designed to be built into the specific application board (26), see Asano (col.9, lines 5-25).

18. As per claim 12 the device according to claim 1, used as a prototyping device to implement a prototype of the specific integrated circuit (27) designed to be built into the specific application board (26), see Asano (col.7, lines 45-54).

19. As per claim 13 the device according to claim 1, used as a development platform for the specific integrated circuit (27) designed to be built into the specified application board (26), see Asano (col.7, lines 45-54, and col.1, lines 59-67).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Itoh et al. Patent No. (6,075,941) microcomputer.
- Watanaba US Patent No. (5,021,996) Device for use in developing and testing a one-chip microcomputer.
- Killian et al. US Patent No. (6,477,683) automated processor generation system for designing a configurable processor and method for the same.
- Reynov et al. US Patent No. (6,668,242) emulator chip package that plugs directly into the target system.
- Phillips et al. US Patent No. (5,321,828) high-speed microcomputer in-circuit emulator.
- Kim, US Pub. No.: US 2002/0116168 A1. Method and system for design verification of electronic circuits.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (703) 605-1372. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (703) 308-6647. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
July 26, 2004

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SUPERVISORY
PATENT EXAMINER